ALEXANDER S. SHERSTINSKY

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JOB OBJECTIVE:

A research position that requires quantitative skills and team work.

EDUCATION:

Massachusetts Institute of Technology:
Sc. D. in Electrical Engineering and Computer Sciences (EECS) with equivalents of minor degrees in Applied Mathematics, Business Administration, and Electronic / Computer Music – June 1994.

Massachusetts Institute of Technology:
S. M. in Electrical Engineering and Computer Sciences – June 1989.

University of California at Berkeley:
B. S. in Electrical Engineering and Computer Sciences – December 1985.

WORK EXPERIENCE:

July 1994 – present

MIT, Cambridge, Massachusetts –
Post-Doctoral Research Fellow at the Media Laboratory: Further M-lattice system research with applications to texture analysis, automatic fingerprint identification systems, secure communications, holography, and computer music.

Sep 1992 – May 1994

MIT, Cambridge, Massachusetts –
Research Assistant at the Media Laboratory: Use of non-linear dynamical systems for analysis and synthesis of visual and sound textures. Doctorate thesis: "M-Lattice: A System For Signal Synthesis And Processing Based On Reaction-Diffusion".
Thesis Supervisor: Professor R. W. Picard.

Summer 1992

HEWLETT-PACKARD Co. (Media Technology Laboratory), Palo Alto, California –
R&D Engineer: Research of statistically-based methods for synthesizing solid textures. Developed a novel information-theoretical approach for efficient representation and synthesis of planar and solid textures.

Winter 1991 and Summer 1991

HEWLETT-PACKARD Co. (Circuit Technology Group R&D), Palo Alto, California joint with HEWLETT-PACKARD Co. (Design Technology Laboratory), Santa Clara, California –
R&D Engineer: Spread awareness of the new multi-chip module (MCM) technology (see below) to various groups at HP, most notably, to the Super-Workstation group and to the Testing group. Surveyed testing methodologies suitable for MCMs and proposed testing strategies. Performed a theoretical yield analysis and modeling for the new MCMs.

Sep 1990 – May 1991

MIT, Cambridge, Massachusetts –
Teaching and Research Assistant in EECS Department: VLSI Design and Computer System Architecture classes. Developing a generalized communications chip for parallel computers.

Summer 1990

HEWLETT-PACKARD Co. (Circuit Technology Group R&D), Palo Alto, California –
R&D Engineer: Research of new type of MCMs. Justified the effort via marketing analysis of VLSI trends. Designed the structure and the fabrication technology for the first prototype of the MCM substrate. Fabricated the samples and performed limited structural testing.

Sep 1989 – May 1990

MIT, Cambridge, Massachusetts –
Teaching and Research Assistant in EECS Department: VLSI Design class. Investigating BiCMOS digital circuits for parallel computers.

June 1989 – Aug 1989

ZYCAD Corporation, Menlo Park, California –
Software Consultant: Design and coding of a spread sheet-like screen editor-translator (10,000 lines of working "C" code) for straight-forward entry and modification of data sheets of various VLSI cell libraries and converting the parameters into formats used by the company's logic simulator.

Mar 1989 – Aug 1989

AT&T, Holmdel, New Jersey –
CAD Software Consultant: Installation, upgrading, and testing of the new SLIC simulator (see below) to fit the needs of the company's VLSI Development Group. The group chose SLIC among several existing simulators to be a part of their new mixed-mode simulator.

Sep 1986 – May 1989

MIT, Cambridge, Massachusetts –
Teaching and Research Assistant in EECS Department: Digital Design & Laboratory and Analog VLSI classes. S. M. thesis titled: "A Programmable Demodulator For Oversampled Analog-To-Digital Modulators". A bi-product of this investigation was a new switch level simulator called "SLIC", whose advantages over some contemporary simulators were: more accurate circuit models, simplicity in usage, and no user intervention.
Thesis Supervisor: Professor C. G. Sodini.

Jan 1986 – Aug 1986

LSI LOGIC, Inc., Palo Alto, California –
Electronic Design Engineer: Design of the ALU portion of LSI Logic's CMOS floating point multiplier-ALU (FPMA) chip. Definition of architecture, block and logic design, behavioral and circuit level simulation, and layout of critical cells. Contributions to the CAD environment for the FPMA project.

May 1985 – Aug 1986

ELECTRONICS RESEARCH LABORATORY, UCB –
Senior Engineering Aide: Design of NMOS ICs for Image Processing applications. Definition of architecture, layout and simulation of modules, and testing of manufactured samples. CAD software contributions to LAGER (a silicon compiler). Wrote a CAD program called "GAME", which generates physical layout from gate-matrix symbolic representation of a circuit.

Summer 1984

HEWLETT-PACKARD Co., Cupertino, California –
Development Engineer: Parametric Gating Plan program (in "BASIC") that implements acceptance / rejection criteria based on values of process-essential parameters for NMOS wafers.

Summer 1983

ELECTRONICS RESEARCH LABORATORY, UCB –
Senior Engineering Aide: Measured processing parameters of KODAK and HUNT photoresists.

Publications

[1] B. Richards, A. Sherstinsky, and R. Brodersen, "A parametrized VLSI video-rate histogram processor," in *Proceedings of IEEE International Conference on Acoustics, Speech and Signal Processing*, vol. 1-13.5, pp. 491–495, Apr. 1987.

[2] A. Sherstinsky and C. G. Sodini, "A Programmable Demodulator for Oversampled Analog-to-Digital Modulators," *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 1092–1103, Sept. 1990.

[3] A. Sherstinsky and R. W. Picard, "On the efficiency of the orthogonal least squares training method for radial basis function networks," Tech. Rep. 271, M.I.T. Media Lab Perceptual Computing Group, Oct. 1993. To Appear in IEEE Transactions on Neural Networks.

[4] A. Sherstinsky and R. W. Picard, "M-Lattice: A novel non-linear dynamical system and its application to halftoning," in *Proceedings of IEEE International Conference on Acoustics, Speech and Signal Processing*, vol. 2, (Adelaide, Australia), pp. 565–568, Apr. 1994.

[5] A. Sherstinsky and R. W. Picard, "Restoration and enhancement of fingerprint images using M-Lattice – a novel non-linear dynamical system," in *Proceedings of International Conference on Pattern Recognition*, (Jerusalem, Israel), Oct. 1994.

[6] A. Sherstinsky and R. W. Picard, "Orientation-sensitive image processing with M-Lattice – a novel non-linear dynamical system," in *Proceedings of First IEEE International Conference on Image Processing*, (Austin, TX), Nov. 1994.

[7] A. Sherstinsky and R. W. Picard, "On stability and equilibria of analog feedback networks," Tech. Rep. 298, M.I.T. Media Lab Perceptual Computing Group, Aug. 1994. Submitted to IEEE Transactions on Circuits and Systems.

[8] A. Sherstinsky and R. W. Picard, "M-lattice: From morphogenesis to image processing," Tech. Rep. 299, M.I.T. Media Lab Perceptual Computing Group, Sept. 1994. Submitted to IEEE Transactions on Image Processing.

[9] A. S. Sherstinsky, "M-Lattice: A System For Signal Synthesis And Processing Based On Reaction-Diffusion," Tech. Rep. 300, M.I.T. Media Lab Perceptual Computing Group, May 1994. Sc.D. Thesis Report.

AFFILIATIONS:

IEEE, Eta Kappa Nu, Tau Beta Pi, Sigma Chi, Toastmasters International.

HOBBIES:

Music (composition and performance), theater (acting), poetry, ice hockey (played varsity and coached intramural, both at MIT), volleyball, skiing, scuba diving, motor boating.

References:

Available upon request.